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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,554	CHEN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. In view of the amendment filed on 03 May 2004, the Examiner withdraws all objections to the specification.

Drawings

2. Corrected drawings have not been received with the current Amendment filed on 03 May 2004 as stipulated in the remarks on page 8.

Claim Objections

3. In view of the amendment filed on 03 May 2004, the Examiner withdraws all objections to the claims.

Response to Arguments

4. Applicant's arguments with respect to amended claims 2 and 6 filed 03 May 2004 have been fully considered but they are not persuasive.

The Applicant contends that Maruyama does not teach "backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation".

The Examiner disagrees and asserts that, in col. 10, lines 29-37, Maruyama explicitly teaches that the simulation is based on forward and backward parts of an integrated circuit so that backtracing can be performed during simulation. In addition, col. 3, lines 30-59 in Maruyama teach that the simulation includes a true-value fault-free simulation component and a fault simulation component for use in comparing results from the simulations and more specifically col. 3, lines 56-59 teach that the simulation takes place by propagating a value from the output pins to the backward circuit portion along observable storage elements, which is a step for backtracing. Furthermore; Figures 19(a)-(c) and col. 23, lines 57-67 in Maruyama give an explicit example of a true-value fault-free simulation/fault simulation whereby circuit elements in Figures 19(a)-(c) are backtraced along the path v-t-p-n-e-d, hence Maruyama explicitly teaches backtracing from each observable node (v-t-p-n-e-d in Figures 19(a)-(c)), said backtrace through each of said internal nodes being based on said fault-free circuit simulation (col. 3, lines 30-59 in Maruyama teach that the backtrace is simulated in both the true-value fault-free simulation and the fault simulation to produce values for a comparison hence the backtrace is based on both the true-value fault-free simulation and the fault simulation; Note: a true-value fault-free simulation is a good machine simulation).

The Applicant contends that Maruyama does not teach that backtracing through observable nodes is "limited to paths along which a faulty value has a possibility of propagating to said observable node".

The Examiner disagrees and asserts that col. 23, lines 6-14 in Maruyama explicitly teaches that the circuit branch point search section in Figure 5 searches the circuit for paths connected to the branch point where a selected fault is assumed to arise to determine a propagation path during backtracing (Note: a branch point is a point at which two or more paths branch from during backtracing; in Figures 19(a)-(c) of Maruyama v, p, s,... are all branches for paths for use in backtracing), hence Maruyama explicitly teaches that backtracing through observable nodes is "limited to paths along which a faulty value has a possibility of propagating to said observable node".

The Examiner disagrees with the Applicants and maintains all rejections to amended claims 2 and 6. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that amended claims 2 and 6 are not patentably distinct or non-obvious over the prior art of record in view of the reference, Maruyama, Daisuke (US 6205567 B1), as applied in the last office action, Paper No. 5. Therefore, the rejection is maintained.

Note: although the Examiner is not changing the grounds of rejection to amended claims 2, 6 and 8-10, the Examiner has rewritten the rejections to reflect changes to claims 2 and 8-10 in the current Amendment filed 03 May 2004 (Note: claim 6 depends from claim 2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 2, 6, 8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Maruyama, Daisuke (US 6205567 B1).

35 U.S.C. 102(e) rejection of claim 2.

Maruyama teaches that in an integrated circuit (IC) having at least one fault to be tested by fault simulation using at least one test (the IC of Figure 8 in Maruyama is an IC having at least one fault to be tested by fault simulation using at least one test; see Abstract in Maruyama; Note: col.1, lines 40-45 in Maruyama teach fault simulation is performed on the basis of the assumption that there will be one fault), each of said tests including at least one input test vector (see Step S2 in Figure 2 of Maruyama), a method for improving the efficiency of the fault simulation (see Abstract in Maruyama) comprising the steps of: a) performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC (col. 14, lines 29-34 in Maruyama teach that a true-value simulation is performed for the i^{th} test; col. 3, lines 42-45 in Maruyama teach that a true-value simulator performs true-value simulation in a

true state-where there is not any fault, i.e. a true value simulation is a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC; col. 14, lines 29-34 in Maruyama teach that the address and true-value for each node are stored in a table in memory; Figure 4 in Maruyama teaches that simulation is performed for each storage element to which a fault event is propagated, i.e., the storage elements are internal nodes of the IC at which faults are detected by comparing the results of the true value simulation with results from the fault simulation; hence Maruyama teaches performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC); b) based on said good machine simulation, identifying faults in said IC that are potentially tested by said at least one test (col. 1, lines 45-48 in Maruyama teach that a list of faults is provided; col. 19, lines 23-25 in Maruyama teach that faults are then injected into the IC during fault simulation; col. 3, lines 45-50 in Maruyama teach that a fault is detected on the basis of a difference between a result of the real-value simulation and a result of the fault simulation; col. 5, lines 63-65 in Maruyama teach that undetectable faults are present in the list of faults; hence the list of faults identify faults that are potentially tested by said at least one test); c) with said at least one test, performing a fault simulation on said faults that were identified as potentially tested (col. 3, lines 45-50 in Maruyama teach that a fault is detected on the basis of a difference between a result of the real-value simulation and a result of the fault simulation); and d) repeating steps a) through c) for each of said at least one test (Figure 2 teaches n tests for repeating steps a to c).

Maruyama teaches backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation (col. 9, lines 37-45 in Maruyama teach backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation; in col. 10, lines 29-37, Maruyama explicitly teaches that the simulation is based on forward and backward parts of an integrated circuit so that backtracing can be performed during simulation; col. 3, lines 30-59 in Maruyama teach that the simulation includes a true-value fault-free simulation component and a fault simulation component for use in comparing results from the simulations and, more specifically, col. 3, lines 56-59 teach that the simulation takes place by propagating a value from the output pins to the backward circuit portion along observable storage elements, which is a step for backtracing; Figures 19(a)-(c) and col. 23, lines 57-67 in Maruyama give an explicit example of a true-value fault-free simulation/fault simulation whereby circuit elements in Figures 19(a)-(c) are backtraced along the path v-t-p-n-e-d, hence Maruyama explicitly teaches backtracing from each observable node (v-t-p-n-e-d in Figures 19(a)-(c)), said backtrace through each of said internal nodes being based on said fault-free circuit simulation) and being limited to paths along which a faulty value has a possibility of propagating to said observable node (col. 5, lines 5-14 in Maruyama teach only paths capable of propagating a faulty value to said observable node are activated; col. 23, lines 6-14 in Maruyama explicitly teaches that the circuit branch point search section in Figure 5 searches the circuit for paths connected to the branch point where a selected fault is assumed to arise, to determine a propagation path during backtracing; Note: a

branch point is a point at which two or more paths branch from during backtracing; in Figures 19(a)-(c) of Maruyama v, p, s,... are all branches for paths for use in backtracing).

35 U.S.C. 102(e) rejection of claim 6.

Col. 5, lines 59-65 in Maruyama teaches that an activation path is activated and becomes able to detect a fault at the time of detection of the fault, hence Maruyama teaches further limiting the number of faults requiring processing by said fault simulation by starting said backtraces from only observable node activation paths wherein a fault was detected (Note: col. 23, lines 6-14 in Maruyama explicitly teaches that the circuit branch point search section in Figure 5 searches the circuit for paths connected to the branch point where a selected fault is assumed to arise, to determine a propagation path during branch activation for backtracing).

35 U.S.C. 102(e) rejection of claim 8.

Maruyama teaches that in an integrated circuit (IC) having at least one fault to be tested by fault simulation using at least one test (the IC of Figure 8 in Maruyama is an IC having at least one fault to be tested by fault simulation using at least one test; see Abstract in Maruyama; Note: col.1, lines 40-45 in Maruyama teach fault simulation is performed on the basis of the assumption that there will be one fault), each of said tests including at least one input test vector (see Step S2 in Figure 2 of Maruyama), a method for improving the efficiency of the fault simulation (see Abstract in Maruyama)

comprising the steps of: a) performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC (col. 14, lines 29-34 in Maruyama teach that a true-value simulation is performed for the i^{th} test; col. 3, lines 42-45 in Maruyama teach that a true-value simulator performs true-value simulation in a true state-where there is not any fault, i.e. a true value simulation is a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC; col. 14, lines 29-34 in Maruyama teach that the address and true-value for each node are stored in a table in memory; Figure 4 in Maruyama teaches that simulation is performed for each storage element to which a fault event is propagated, i.e., the storage elements are internal nodes of the IC at which faults are detected by comparing the results of the true value simulation with results from the fault simulation; hence Maruyama teaches performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC); b) based on said good machine simulation, identifying faults in said IC that are blocked by said at least one test from being observed at an observable point of said IC (col. 11, lines 19-25 of Maruyama teach a flag for indicating undetected faults; Note: undetected faults are blocked faults); c) with said at least one test, performing a fault simulation on said faults that were identified as not being blocked (col. 3, lines 45-50 in Maruyama teach that a fault is detected on the basis of a difference between a result of the real-value simulation and a result of the fault simulation; Note: only a detectable or non-blocked fault can propagate a result of the fault simulation that would make the fault detectable); and d) repeating

steps a) through c) for each of said at least one test (Figure 2 teaches n tests for repeating steps a to c).

Maruyama teaches backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation (col. 9, lines 37-45 in Maruyama teach backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation; in col. 10, lines 29-37, Maruyama explicitly teaches that the simulation is based on forward and backward parts of an integrated circuit so that backtracing can be performed during simulation; col. 3, lines 30-59 in Maruyama teach that the simulation includes a true-value fault-free simulation component and a fault simulation component for use in comparing results from the simulations and, more specifically, col. 3, lines 56-59 teach that the simulation takes place by propagating a value from the output pins to the backward circuit portion along observable storage elements, which is a step for backtracing; Figures 19(a)-(c) and col. 23, lines 57-67 in Maruyama give an explicit example of a true-value fault-free simulation/fault simulation whereby circuit elements in Figures 19(a)-(c) are backtraced along the path v-t-p-n-e-d, hence Maruyama explicitly teaches backtracing from each observable node (v-t-p-n-e-d in Figures 19(a)-(c)), said backtrace through each of said internal nodes being based on said fault-free circuit simulation) and being limited to paths along which a faulty value has a possibility of propagating to said observable node (col. 5, lines 5-14 in Maruyama teach only paths capable of propagating a faulty value to said observable node are activated; col. 23, lines 6-14 in Maruyama explicitly teaches that the circuit branch point search section in

Figure 5 searches the circuit for paths connected to the branch point where a selected fault is assumed to arise, to determine a propagation path during backtracing; Note: a branch point is a point at which two or more paths branch from during backtracing; in Figures 19(a)-(c) of Maruyama v, p, s,... are all branches for paths for use in backtracing).

35 U.S.C. 102(e) rejection of claim 11.

Col. 5, lines 59-65 in Maruyama teaches that an activation path is activated and becomes able to detect a fault at the time of detection of the fault, hence Maruyama teaches further limiting the number of faults requiring processing by said fault simulation by starting said backtraces from only observable node activation paths wherein a fault was detected (Note: col. 23, lines 6-14 in Maruyama explicitly teaches that the circuit branch point search section in Figure 5 searches the circuit for paths connected to the branch point where a selected fault is assumed to arise, to determine a propagation path during branch activation for backtracing).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama, Daisuke (US 6205567 B1).

35 U.S.C. 103(a) rejection of claim 9.

Claim 9 is a software implementation of the limitations in claim 8 containing all of the limitations of claim 8 except for the software implementation of those limitations.

Maruyama, substantially teaches the claimed invention described in claim 8 (as rejected above).

However Maruyama, does not explicitly teach the specific use of a software implementation for the limitations in claim 8.

The Examiner asserts that use of a software implementation for the limitations in claim 8 versus a hardware implementation for the limitations in claim 8 or any combination thereof would have been based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Maruyama by including use of a software implementation for the limitations in claim 8. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a software implementation for the limitations in claim 8 would have provided the opportunity to implement the test device in the Maruyama patent based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

35 U.S.C. 103(a) rejection of claim 10.

Claim 10 is a software implementation of the limitations in claim 1 containing all of the limitations of claim 1 except for the software implementation of those limitations. Maruyama, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Maruyama, does not explicitly teach the specific use of a software implementation for the limitations in claim 1.

The Examiner asserts that use of a software implementation for the limitations in claim 1 versus a hardware implementation for the limitations in claim 1 or any combination thereof would have been based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is

generally faster than software) and flexibility (Note: software is more flexible than hardware).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Maruyama by including use of a software implementation for the limitations in claim 1. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a software implementation for the limitations in claim 1 would have provided the opportunity to implement the test device in the Maruyama patent based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

35 U.S.C. 103(a) rejection of claim 12.

Col. 5, lines 59-65 in Maruyama teaches that an activation path is activated and becomes able to detect a fault at the time of detection of the fault, hence Maruyama teaches further limiting the number of faults requiring processing by said fault simulation by starting said backtraces from only observable node activation paths wherein a fault was detected (Note: col. 23, lines 6-14 in Maruyama explicitly teaches that the circuit branch point search section in Figure 5 searches the circuit for paths connected to the branch point where a selected fault is assumed to arise, to determine a propagation path during branch activation for backtracing).

35 U.S.C. 103(a) rejection of claim 13.

Col. 5, lines 59-65 in Maruyama teaches that an activation path is activated and becomes able to detect a fault at the time of detection of the fault, hence Maruyama teaches further limiting the number of faults requiring processing by said fault simulation by starting said backtraces from only observable node activation paths wherein a fault was detected (Note: col. 23, lines 6-14 in Maruyama explicitly teaches that the circuit branch point search section in Figure 5 searches the circuit for paths connected to the branch point where a selected fault is assumed to arise, to determine a propagation path during branch activation for backtracing).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2133